

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: **Taketo WATANABE, et al.**

Serial Number: **Not Yet Assigned**

Filed: **August 5, 2003**

For: **SEMICONDUCTOR DEVICE, MANUFACTURING METHOD THEREOF, AND CMOS INTEGRATED CIRCUIT DEVICE**

**INFORMATION DISCLOSURE STATEMENT**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

August 5, 2003

Sir:

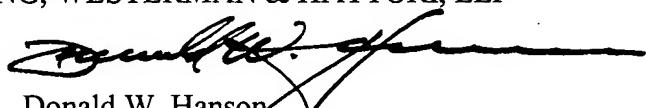
In compliance with 37 CFR 1.56, Applicants call to the attention of the Patent and Trademark Office the reference listed on the attached PTO-1449.

A copy of the reference is enclosed herewith.

In the event there are any fees due in connection with the filing of this paper, please charge  
Deposit Account No. 01-2340.

Respectfully submitted,

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PATENT TRADEMARK OFFICE

Enclosures: PTO-1449; References (1)

<b>INFORMATION DISCLOSURE STATEMENT PTO-1449</b>	Atty. Docket No. 030927	Serial No. New Application
Applicant(s): Taketo WATANABE, et al.		
	Filing Date: August 5, 2003	Group Art Unit: Not Yet Assigned

#### U.S. PATENT DOCUMENTS

Examiner Initial	Document No.	Name	Date	Class	Subclass	Filing Date (If appropriate)
_____	AA					
_____	AB					
_____	AC					
_____	AD					

#### FOREIGN PATENT DOCUMENTS

	Document No.	Date	Country	Translation (Yes or No)
_____	AE	6-37309	02/10/94	Japan
_____	AF			Yes-Discussed in the specification
_____	AG			
_____	AH			
_____	AI			

#### OTHER DOCUMENTS

_____	AJ	
_____	AK	
Examiner	Date Considered	